

Fig 1A

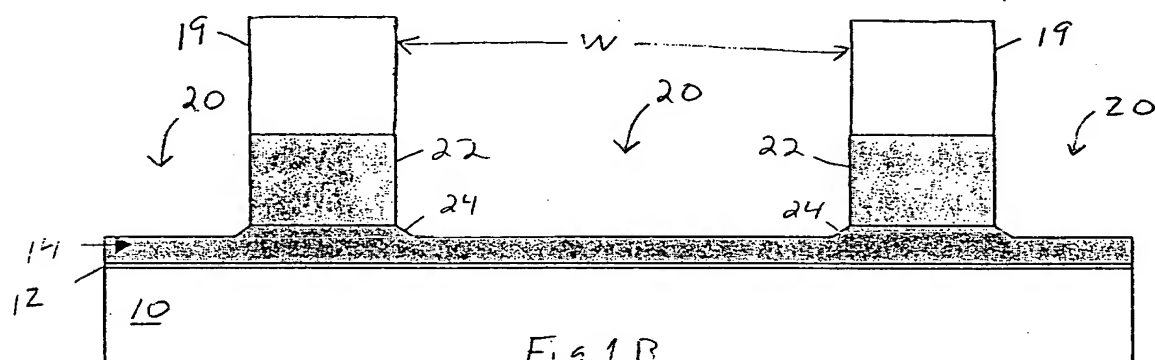


Fig 1B

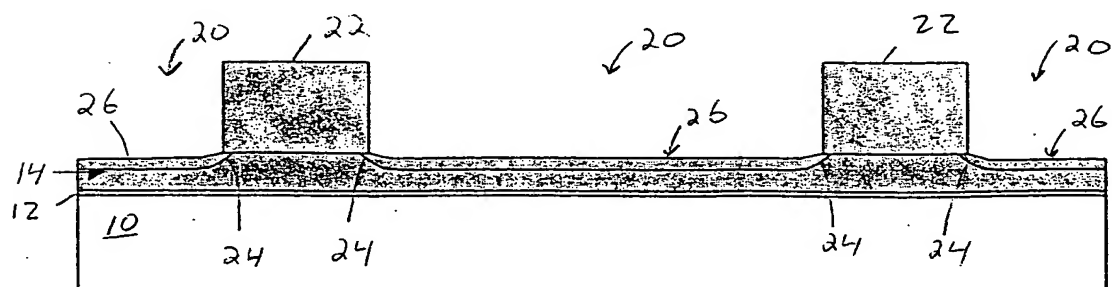


Fig 1C

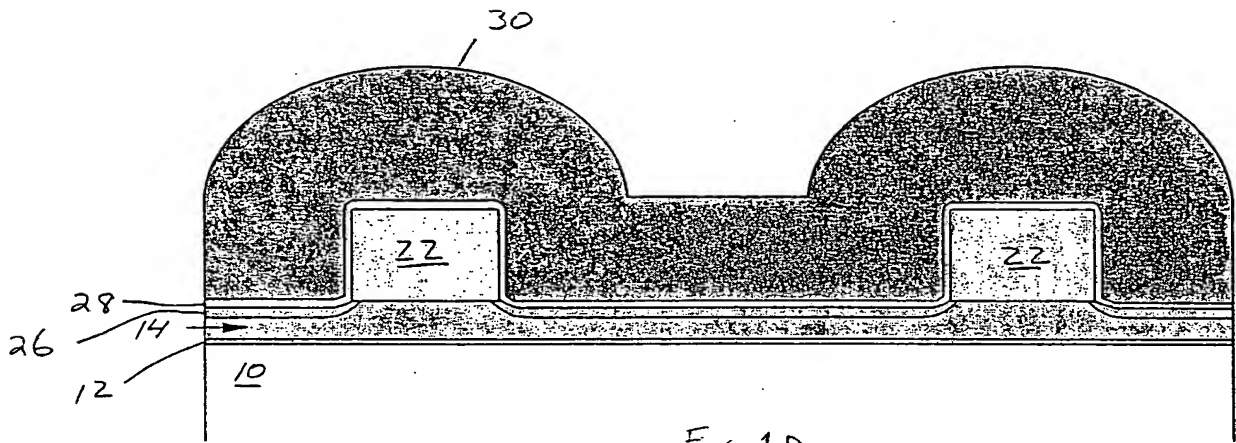


Fig 1D

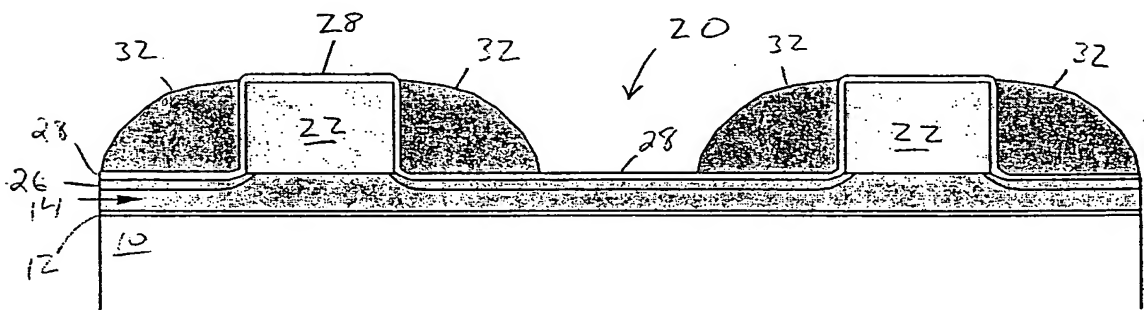
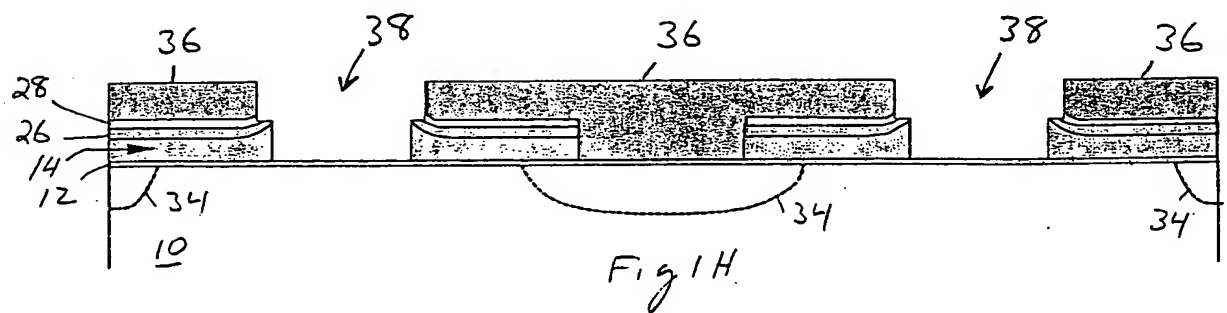
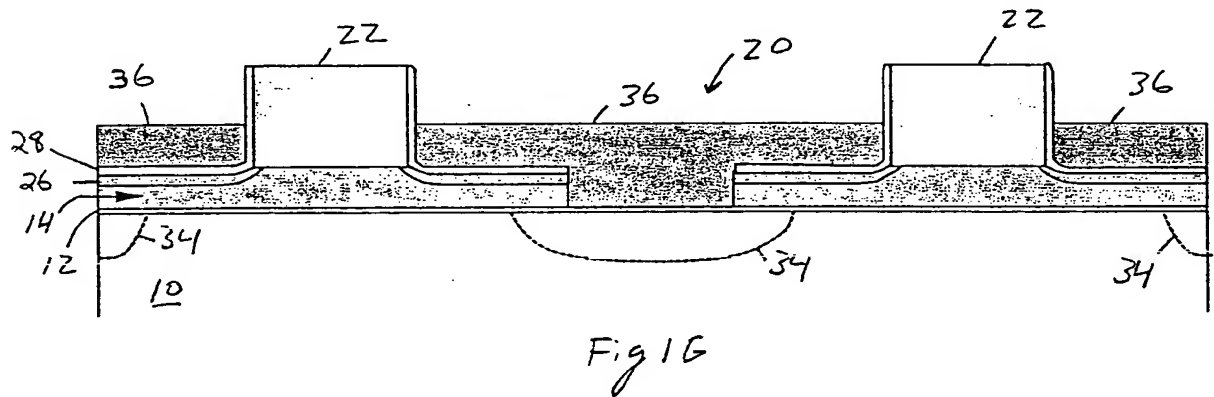
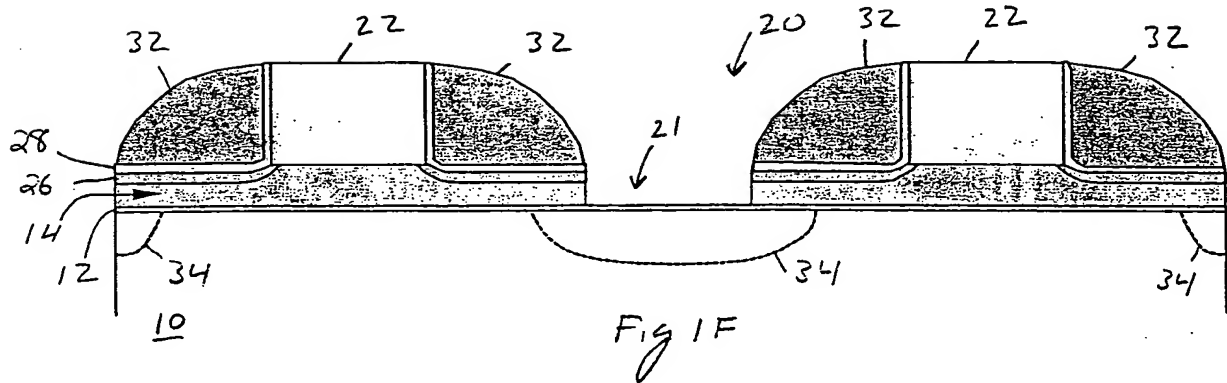
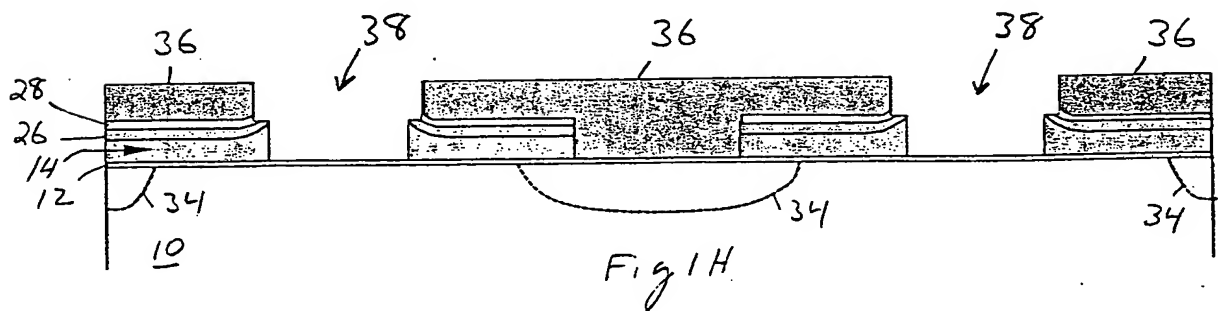
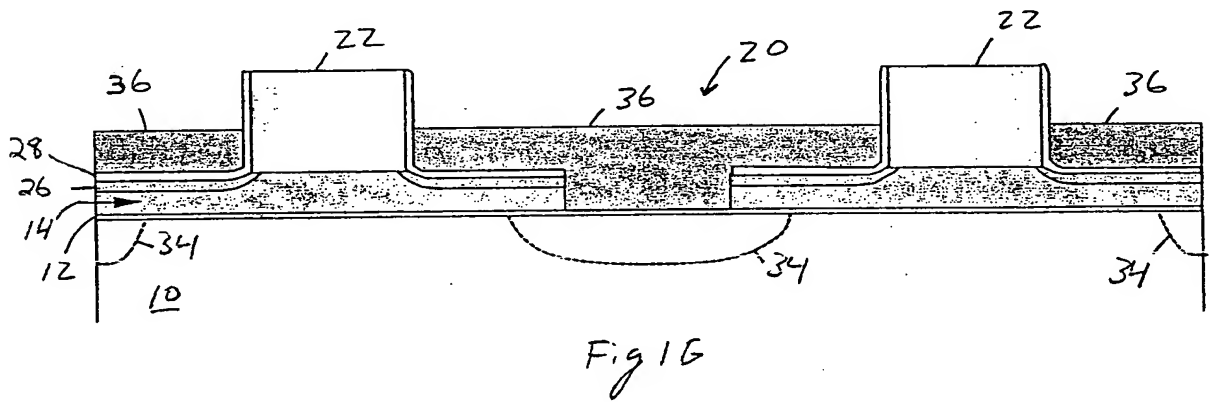
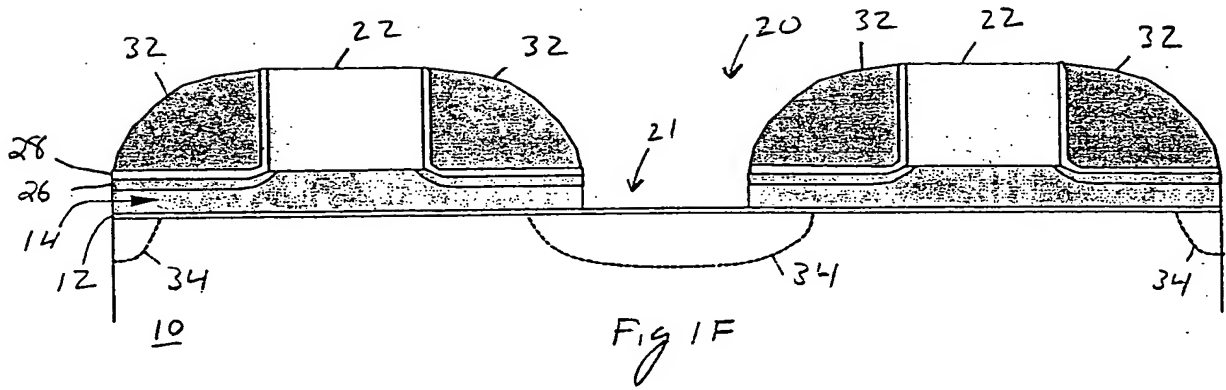
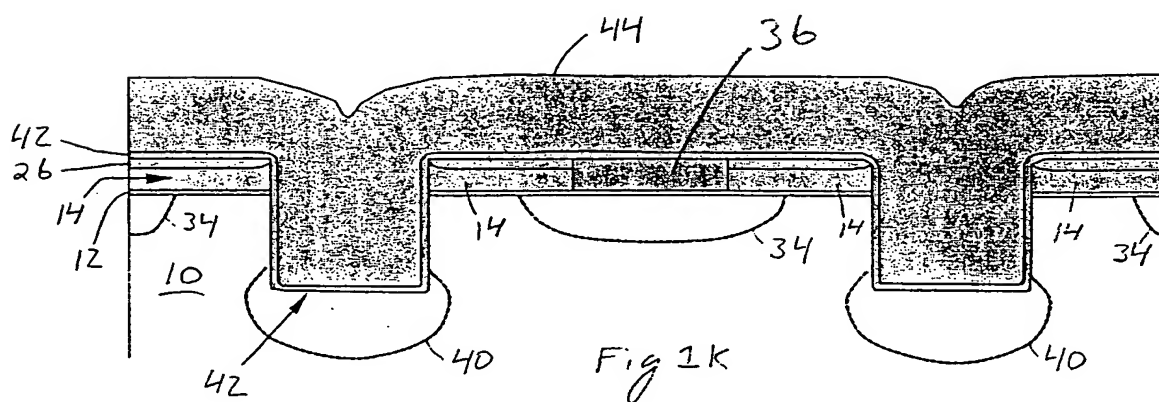
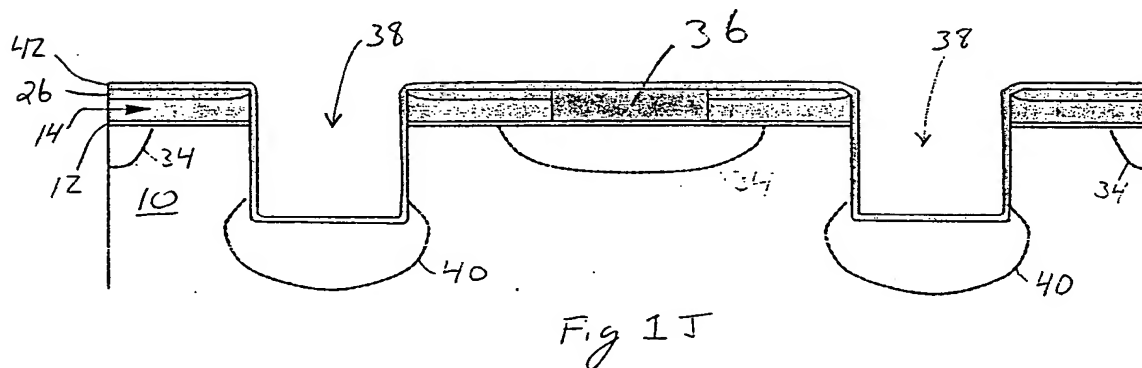
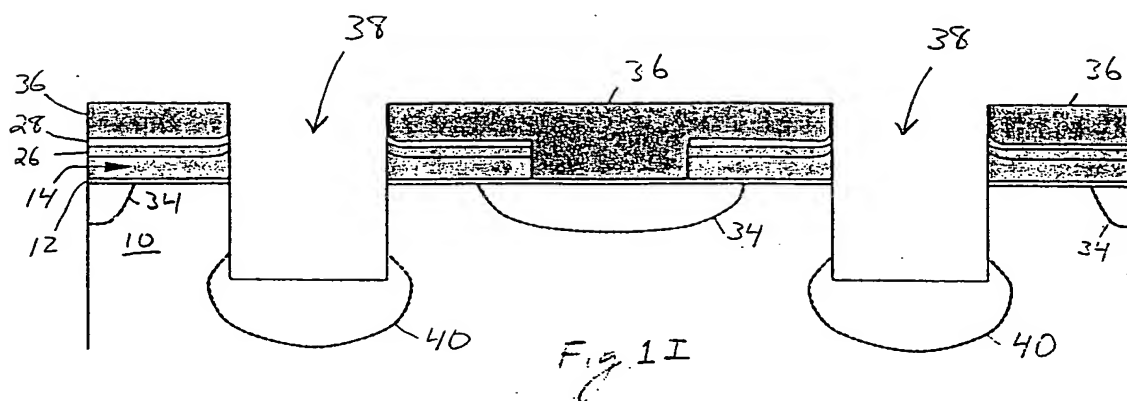
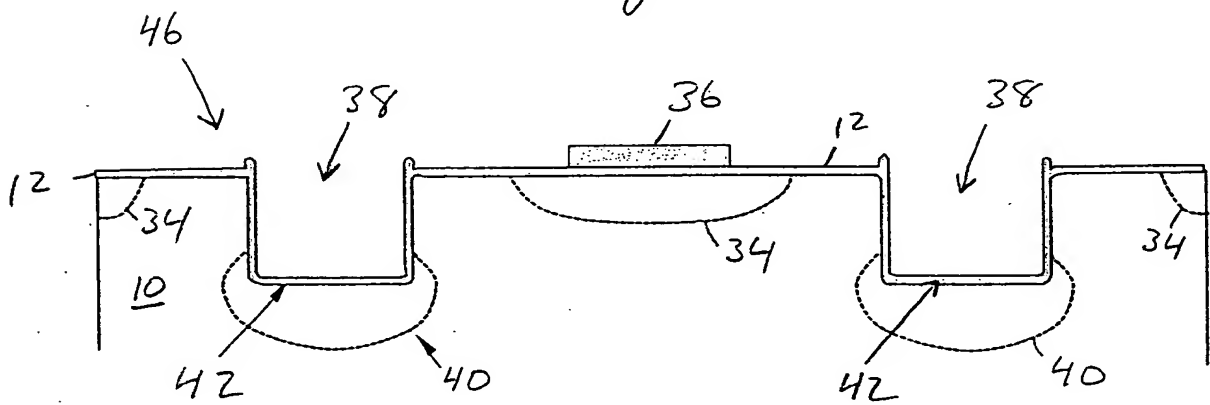
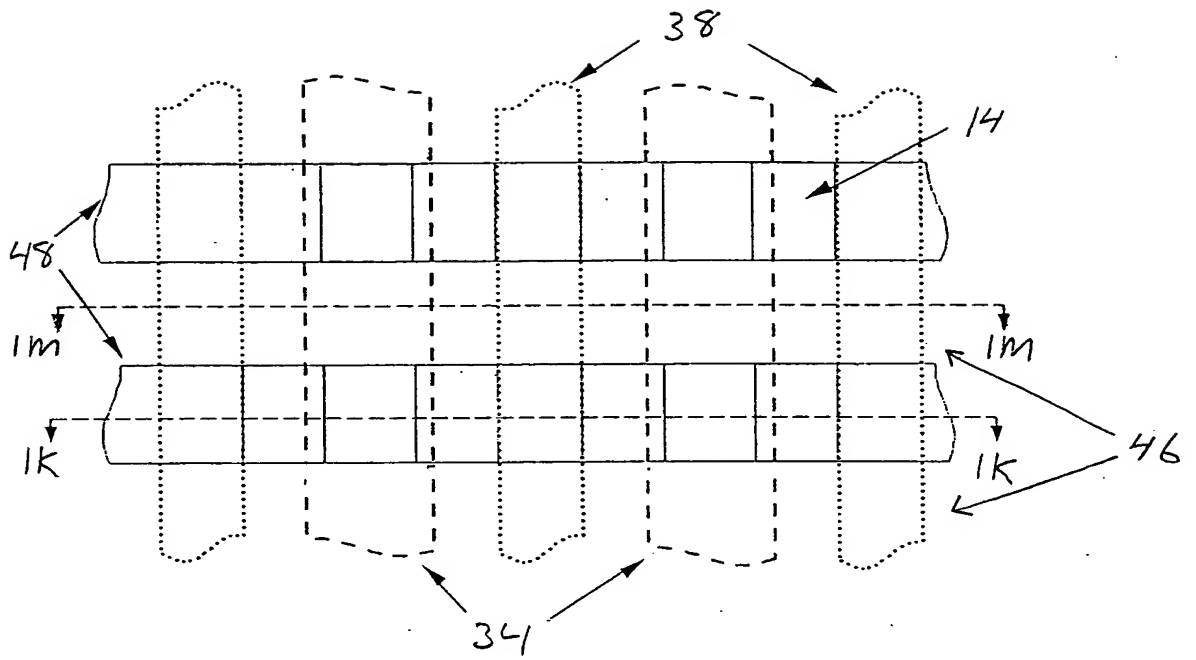


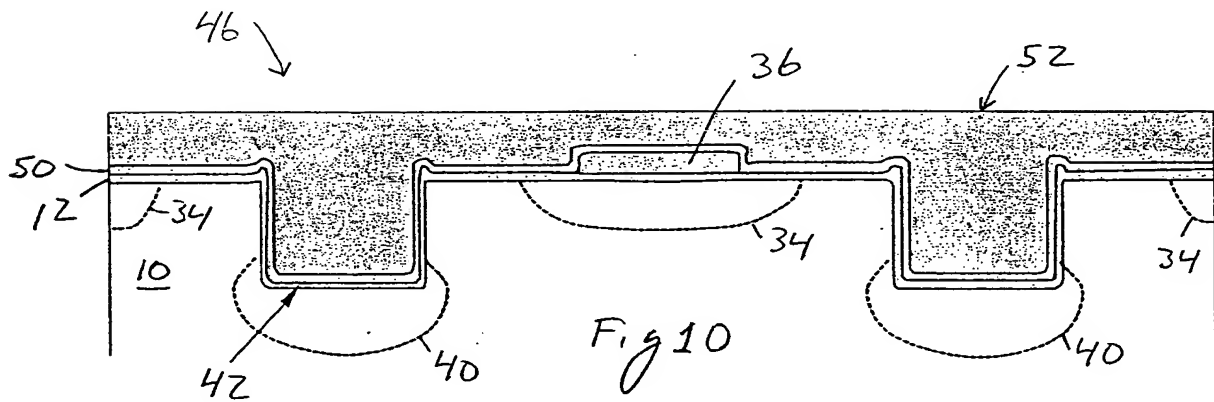
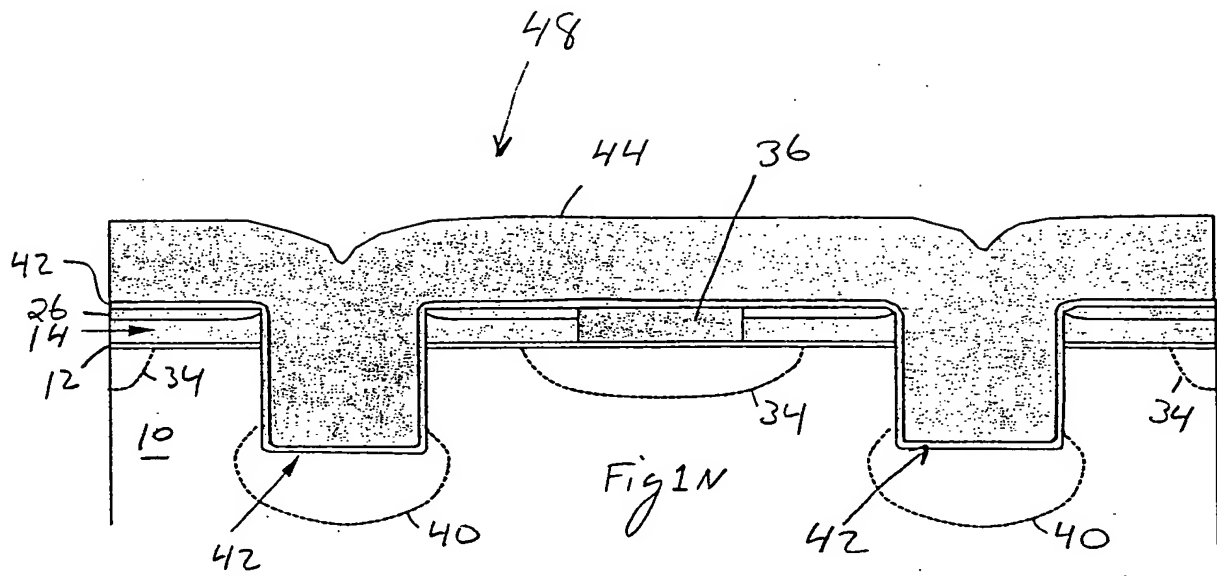
Fig 1E











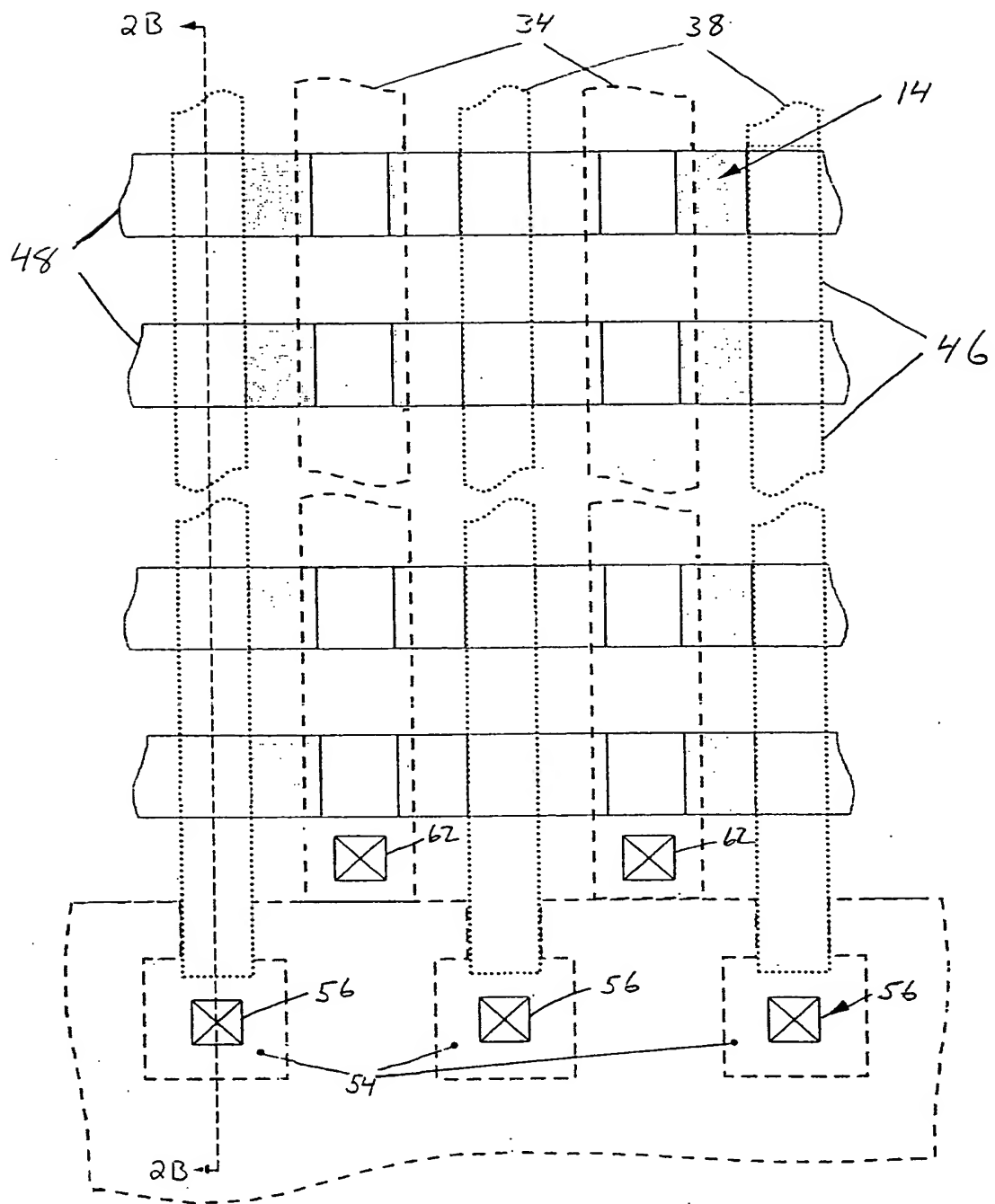


Fig 2A

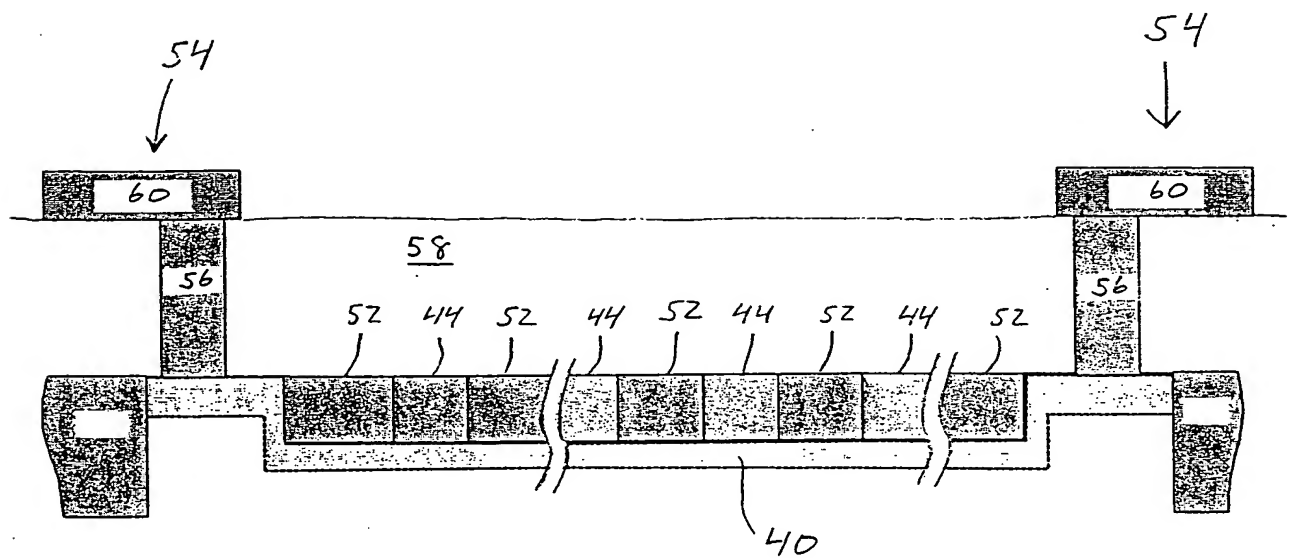


Fig 2B

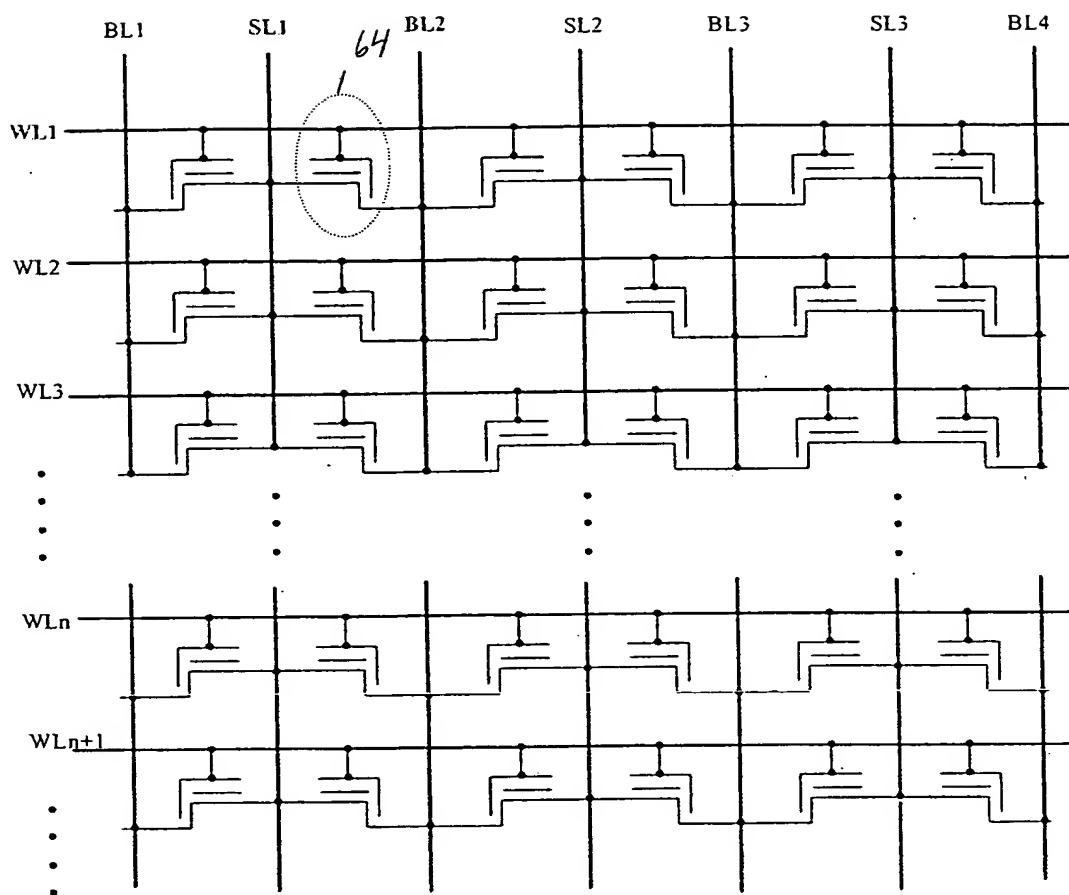


Fig 3

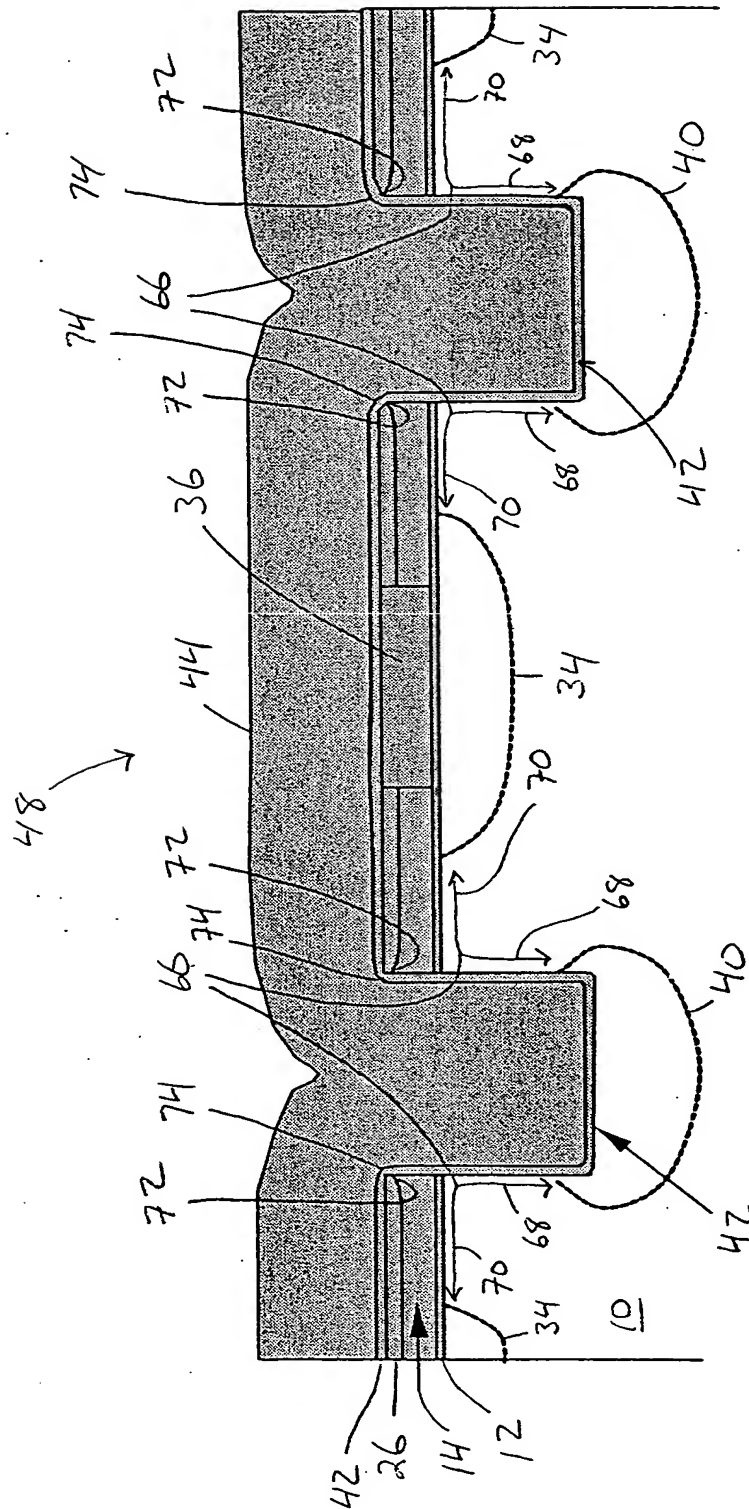
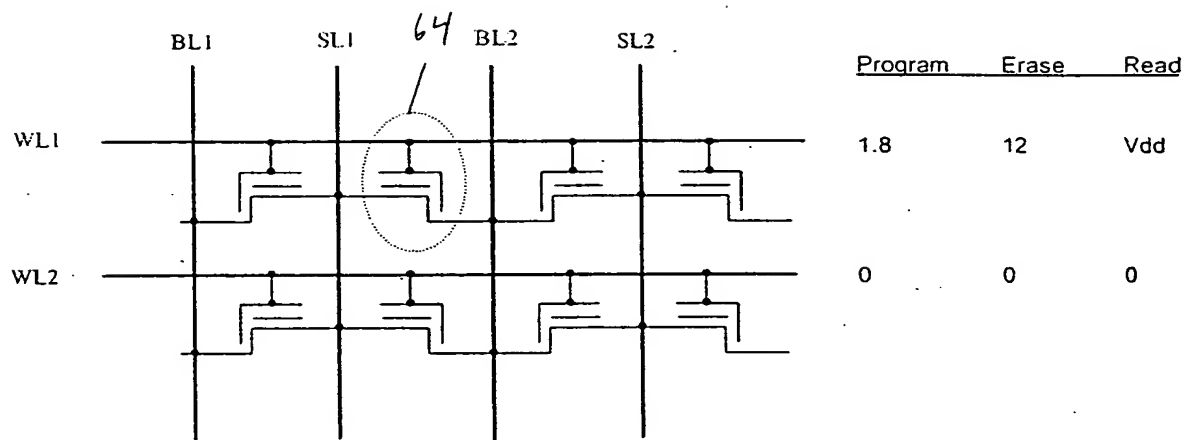


Fig 4



Program	Vdd (inhibit)	Vpp (e.g. 9-10V)	Vdp (0.5-1V)	0 (inhibit)
Erase	0	0	0	0
Read	0	0	-1V	0

Fig 5

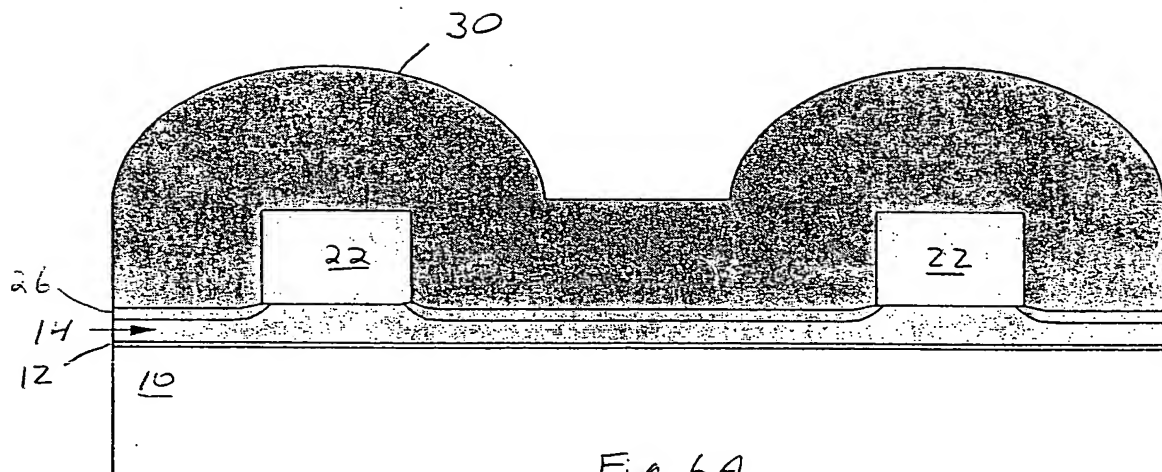


Fig 6A

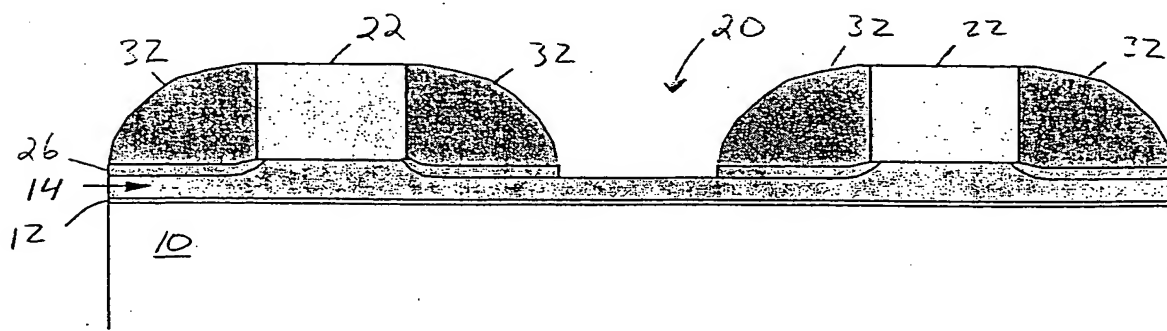
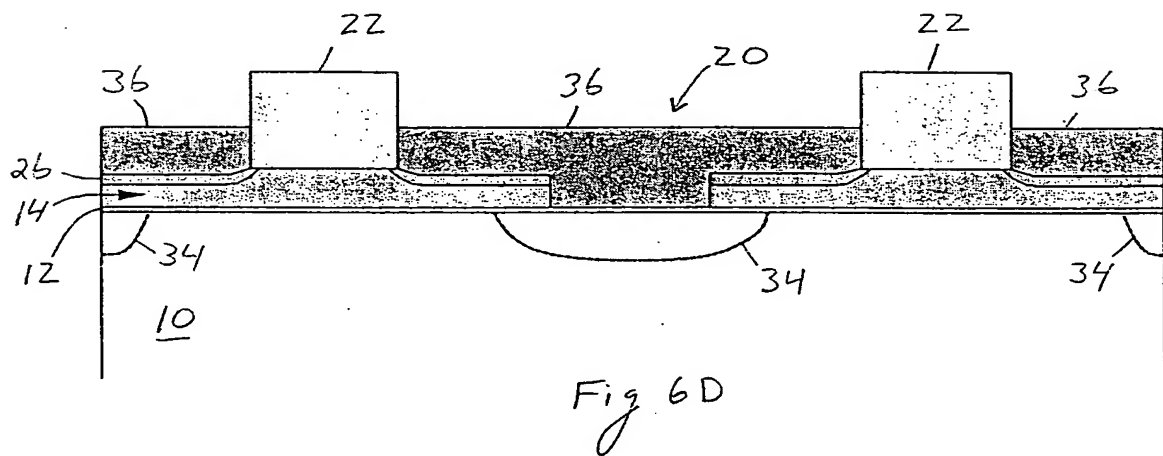
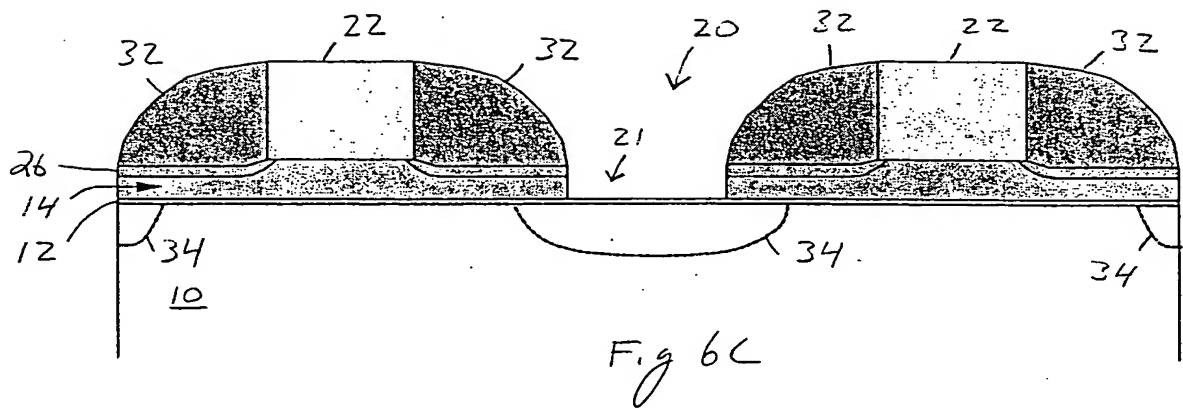


Fig 6B



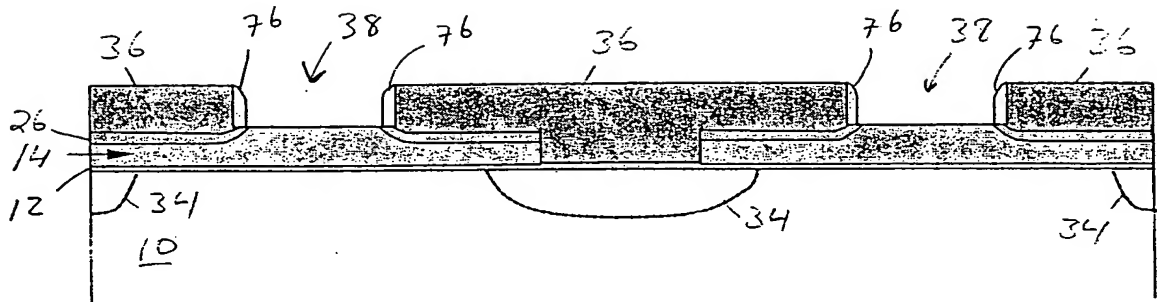


Fig 6E

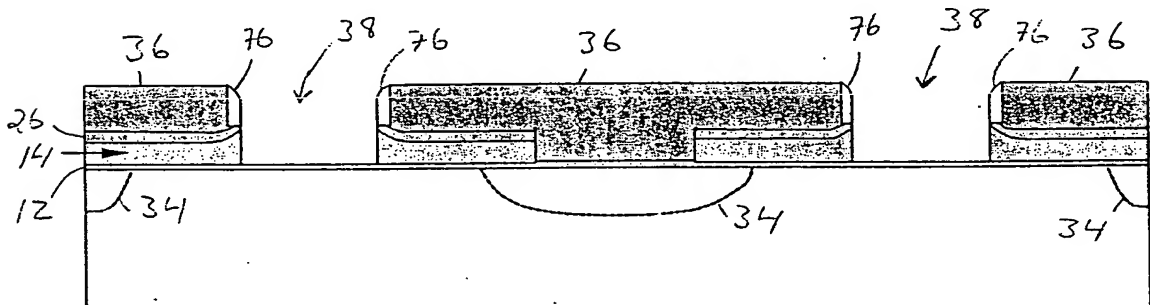


Fig 6F

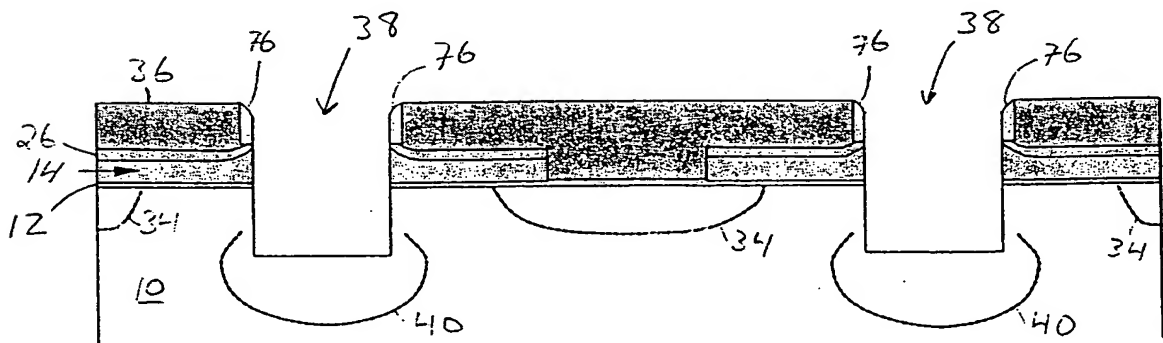


Fig 6G

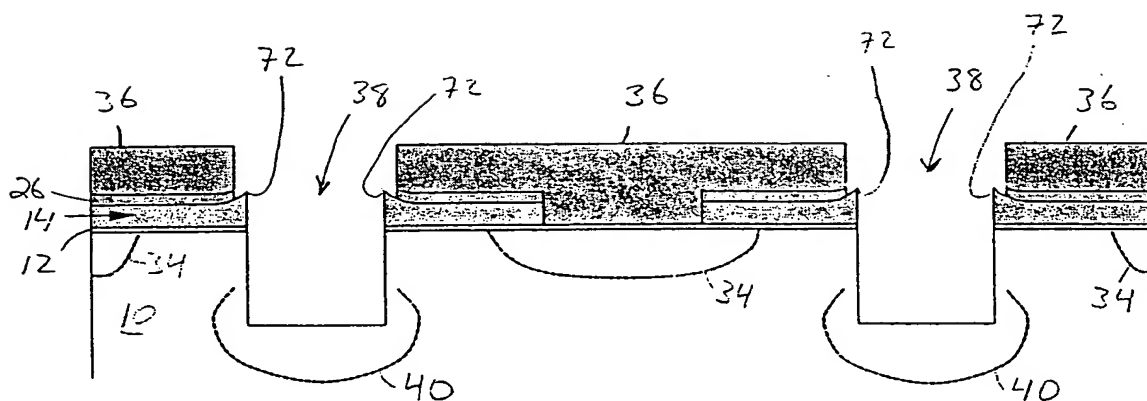


Fig 6H

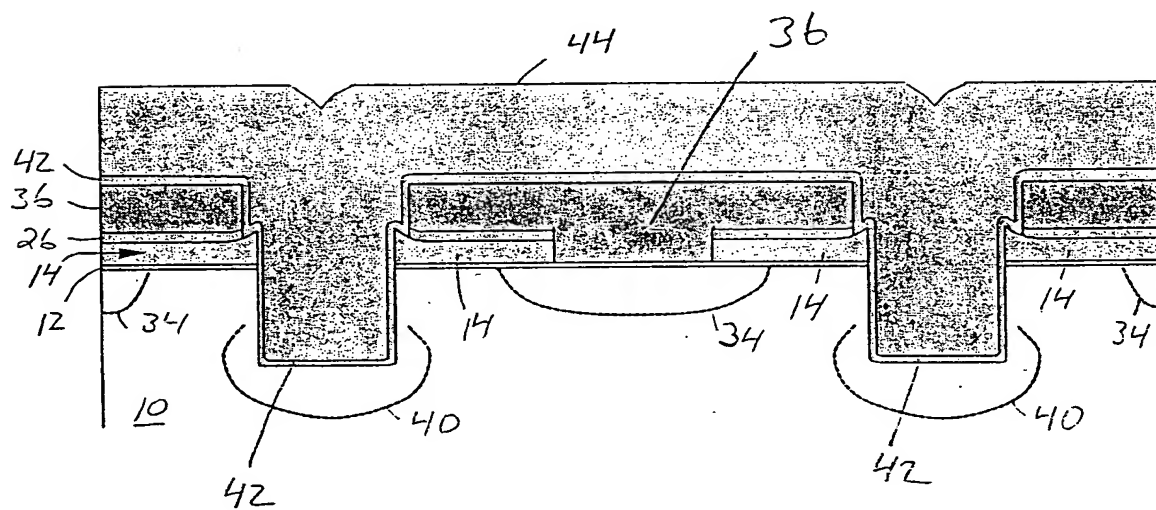
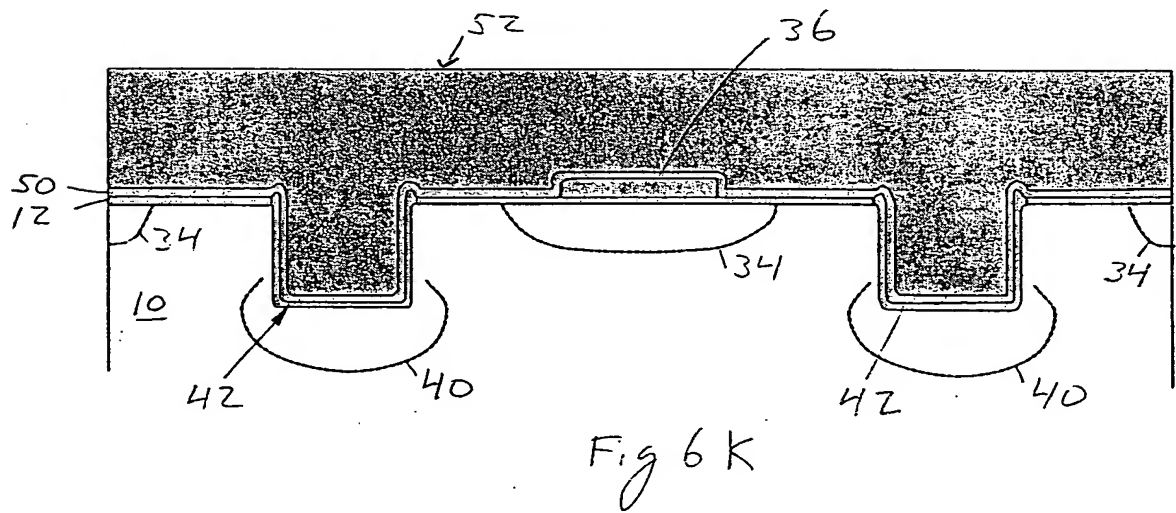
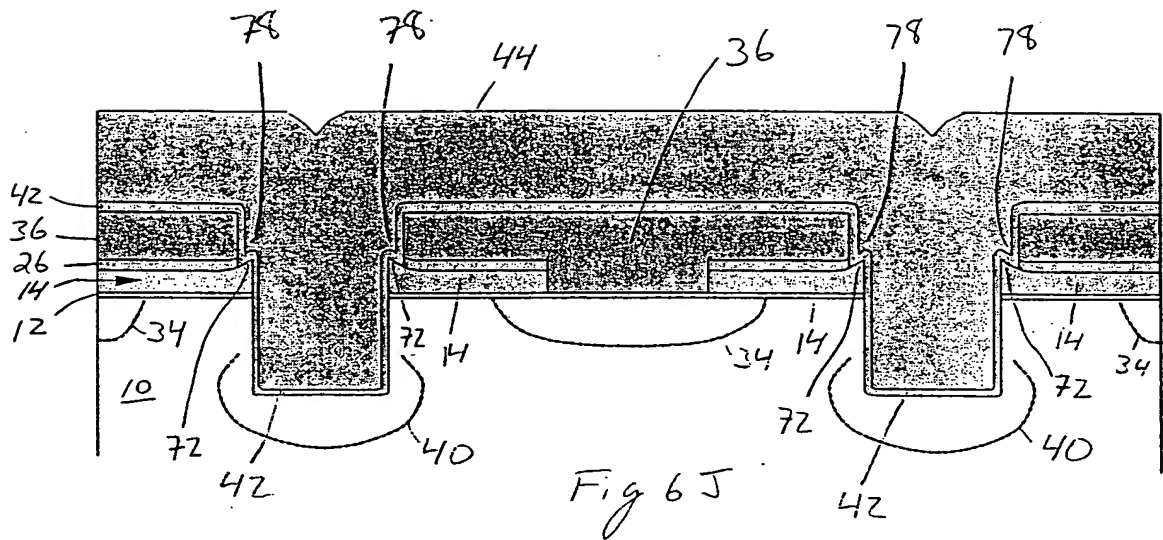


Fig 6 I



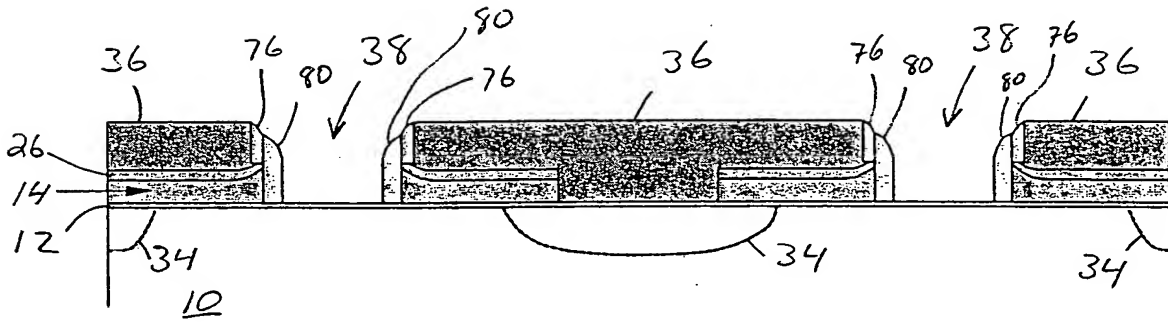


Fig 7A

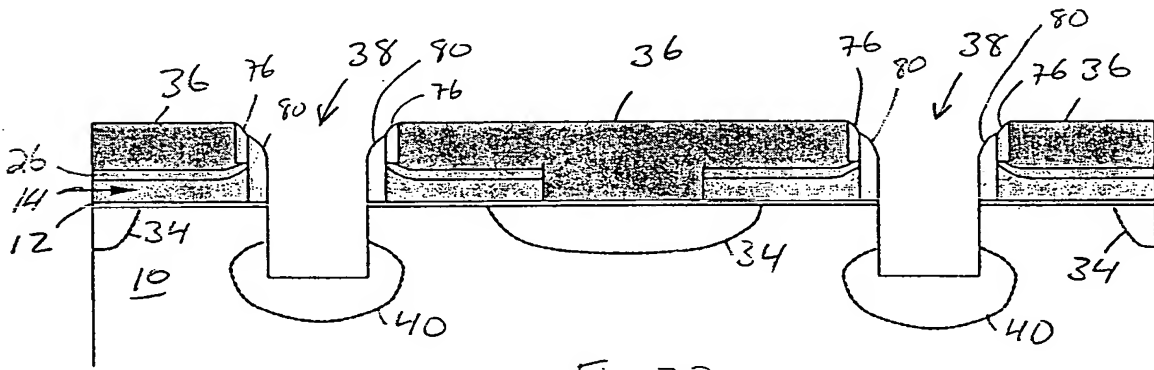


Fig 7B

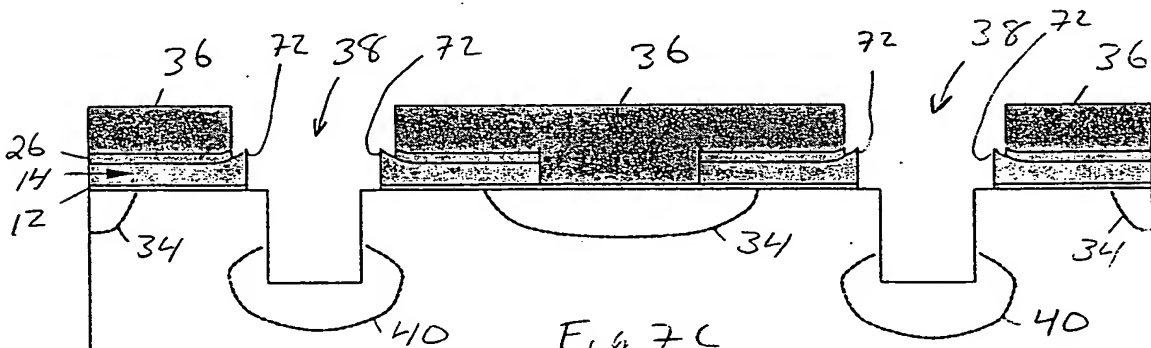


Fig 7C

